Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **D1**
2. **D3**
3. **S3**
4. **S4**
5. **D4**
6. **D2**
7. **S2**
8. **IN2**
9. **V+**
10. **VL**
11. **GND**
12. **V-**
13. **IN1**
14. **IN1**
15. **S1**

**2**

**3**

**4**

**5**

**1 14**

**13**

**12**

**11**

**10**

**9**

**8**

**6 7**

**.085”**

**.068”**

**50843A**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” min.**

**Backside Potential:**

**Mask Ref: 50843A**

**APPROVED BY: DK DIE SIZE .068” X .085” DATE: 3/9/23**

**MFG: INTERSIL SEMI THICKNESS .019” P/N: DG403**

**DG 10.1.2**

#### Rev B, 7/19/02